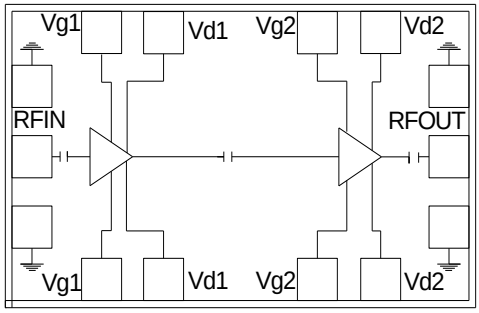
5.3 – 6.5 GHz 1 Watt Power Amplifier

Features

- **Frequency Range : 5.3 – 6.5 GHz**
- **30.5 dBm Psat**
- **17 dB Power gain**
- **25% PAE**
- **High IP3**
- **Input Return Loss > 15 dB**
- **Output Return Loss > 12 dB**
- **Dual bias operation**
- **No external matching required**
- **DC decoupled input and output**
- **0.5 µm InGaAs pHEMT Technology**
- **Chip dimension: 2.0 x 1.0 x 0.1 mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

Description

The ASL4011 is a C-band Power amplifier with 30.5 dBm power output. The PA uses 2 stages of amplification and operates in 5.3 – 6.5 GHz frequency range. It features 17 dB of gain. It has a high IP3 of 40dBm and 25% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage.The die is fabricated using a reliable 0.5µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+10	volts
Drain current (Id)	0.6	A
RF input power (RFin at Vd=8V)	33	dBm
Operating temperature	-50 to +85	°C
Storage Temperature	-65 to +150	°C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications (1) @ T_A = 25 °C, V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -1.1V Z_o =50 Ω

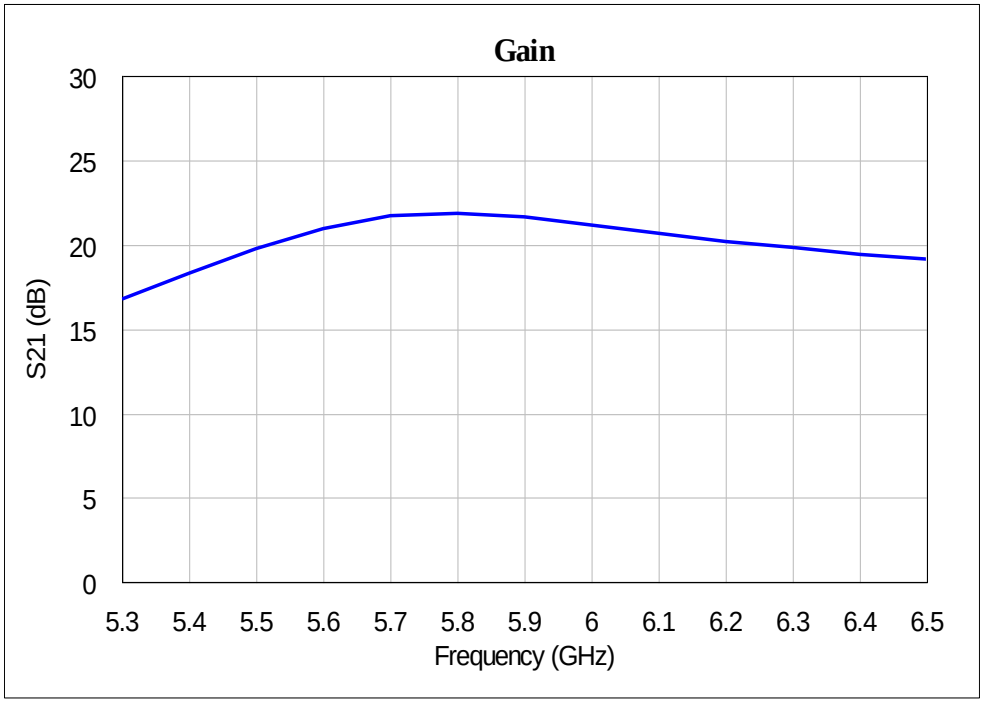
Parameter	Typ.	Units
Frequency Range	5.3 – 6.5	GHz
Gain	17 (min)	dB
Output Power (P1 dB)	29.5	dBm
Input Return Loss	15	dB
Output Return Loss	15	dB
Saturated output power (Psat)	30.5	dBm
Output Third Order Intercept (IP3)	40	dBm
Power Added Efficiency (PAE)	25%	--
Supply Current(I_{dq})	330	mA
Supply Current(I_{dsat}[2])	450	mA

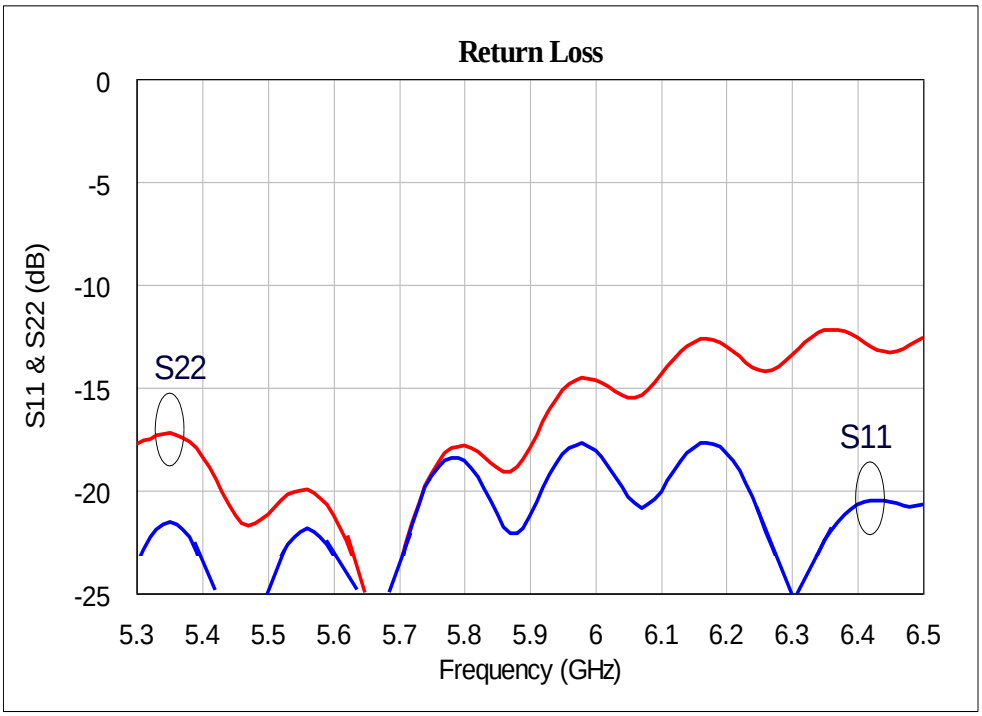
Note:

1. Electrical specifications as measured in test fixture.
2. I_{dsat} is the maximum current under input RF drive condition.

Test fixture data

V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -1.1V, Total Current (Idq) =330mA, T_A = 25 °C





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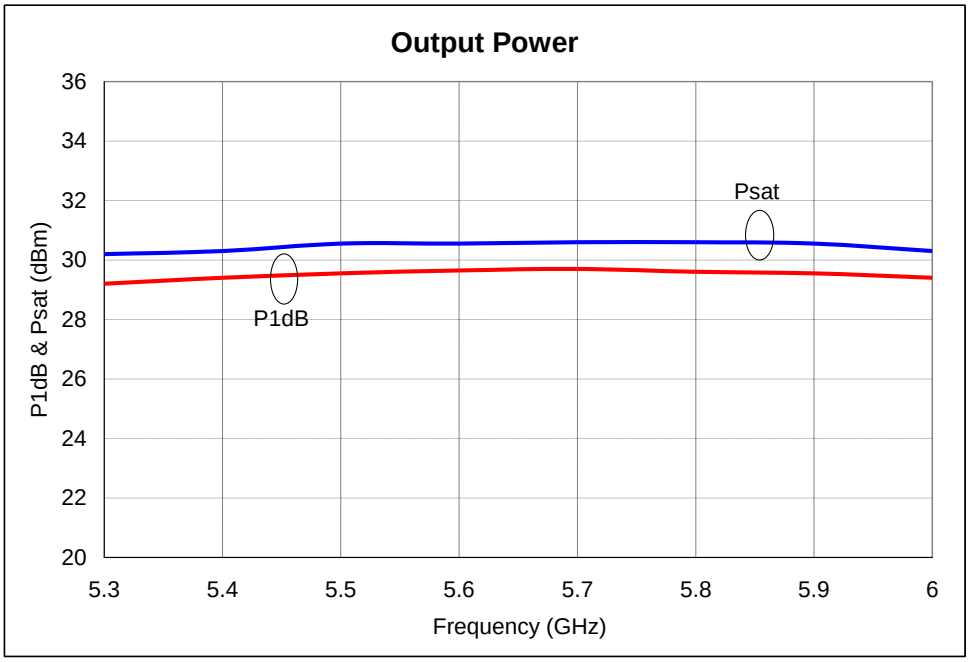
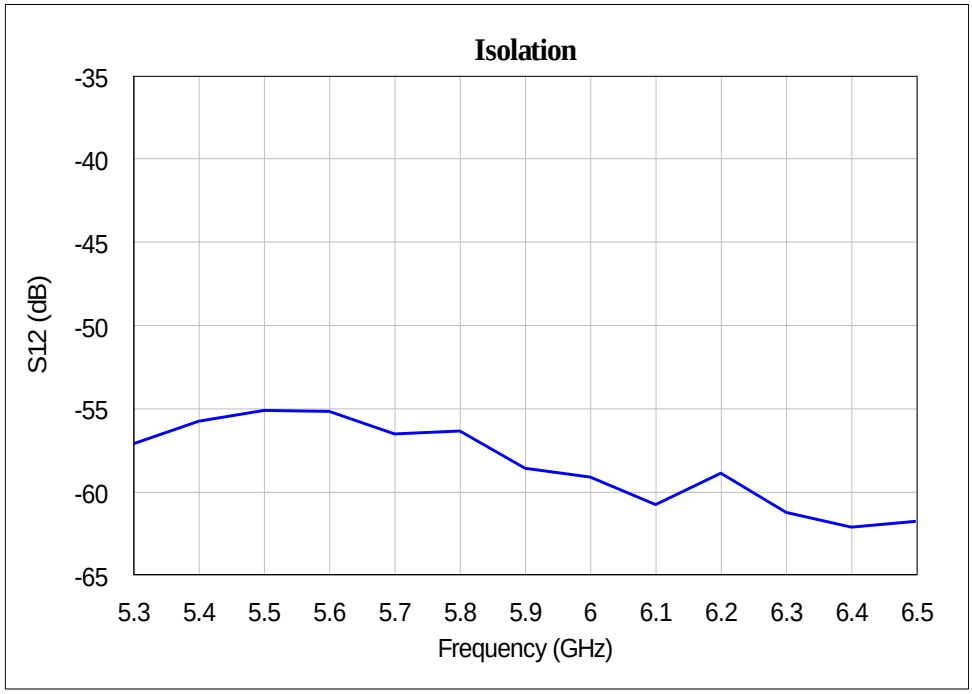
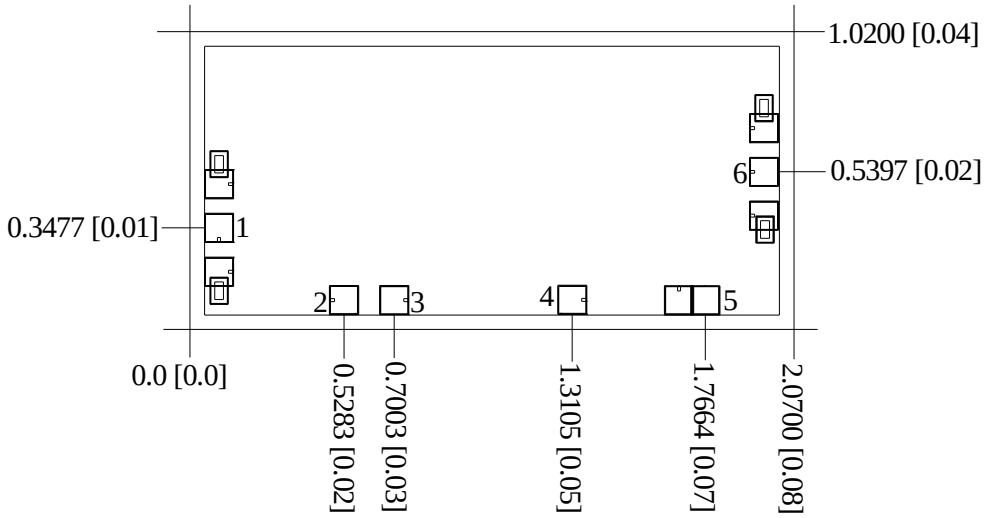




Bond Pad Locations

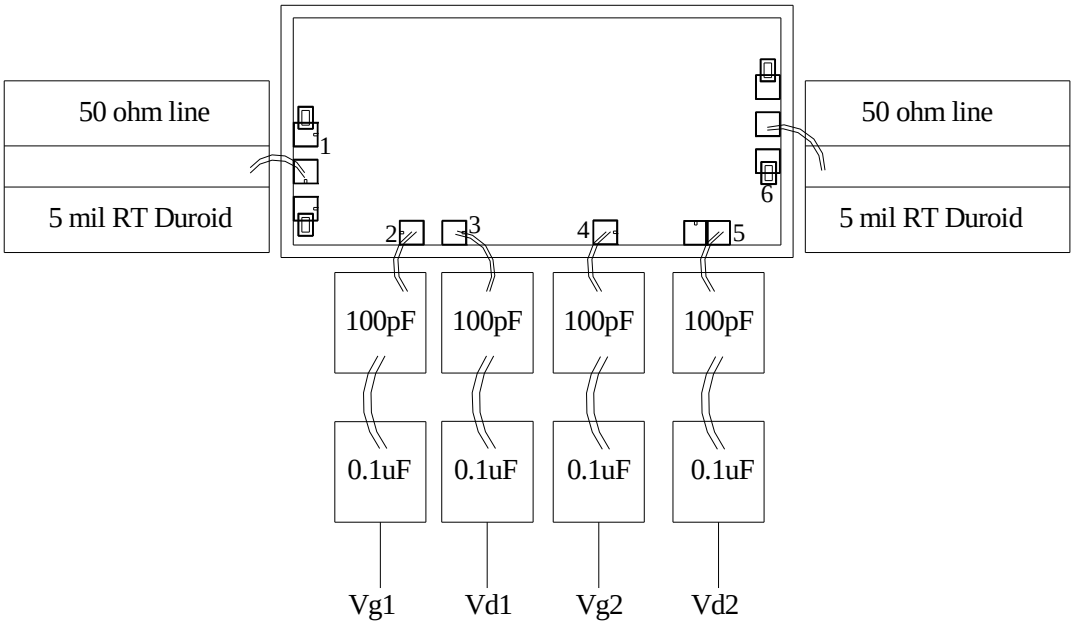


Units: millimeters (inches)

Note:

1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 2 : 1st stage gate voltage(V_{g1})
4. Pad no. 6 : RF Output
5. Pad no. 3 : 1st stage drain voltage(V_{d1})
6. Pad no. 4 : 2nd stage gate voltage(V_{g2})
7. Pad no. 5 : 2nd stage drain voltage (V_{d2})
8. All the dimensions shown above are measured taking bottom left corner as reference.

Recommended Assembly Diagram



Note :

1. Open stub of 4mm length and 1mm width to be placed at output for matching.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
3. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF capacitor.
4. Input and output 50 ohm lines are on 5 mil RT Duroid substrate.
5. 0.1uF and 1uFcapacitors can be additionally used for effective bypass.
6. The RF input & output ports are DC decoupled on-chip.
7. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip.

Die attach: For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice